CLAIMS:

1.   A watchdog system for monitoring functionality of a processor, the system comprising:

control logic having N number of acknowledgement signal inputs;

a first timer, wherein said first timer is started upon boot up of said watchdog system;

a second timer;

a third timer, wherein said second and third timers are started upon receiving a first acknowledgement signal at one of said N number of acknowledgement signal inputs; and

a reset signal generator.

2.   The watchdog system of claim 1, wherein said reset signal generator generates a reset signal upon any one of the following conditions being met:

(i) not receiving an acknowledgement signal at one of said N number of acknowledgement signal inputs before an expiration of said first timer, (ii) receiving an acknowledgement signal at one of said N number of acknowledgement signal inputs before an expiration of said second timer; and (iii) not receiving an acknowledgement signal at all of said N number of acknowledgement signal inputs before an expiration of said third timer.

3.   The watchdog system of claim 1, further comprising an interface coupled to said control logic via said N number of acknowledgement signal inputs, wherein said interface couples said processor to said watchdog system.

4.   The watchdog system of claim 3, wherein said reset signal resets said processor coupled to said processor interface.

5.   The watchdog system of claim 4, further includes logic to save information pertaining to a state of said processor immediately prior to reset.

6.   The watchdog system of claim 1, wherein a duration of each of said timers can be set to unique values.

7.   The watchdog system of claim 1, wherein said N number of acknowledgement signal inputs are input/output lines.

8.   The watchdog system of claim 1, wherein said N number of acknowledgement signal inputs are registers.

9.   A method of monitoring functionality of a processor comprising the steps of:

starting a first timer;

starting a second timer,

receiving at least one acknowledgement signal from a processor or software module;

upon the reception of every one of at least one acknowledgement signal, restarting

said first timer; and

resetting said processor if any one of the following conditions are met:

(i) receiving any one of said at least one acknowledgement signal prior to an expiration of said first timer and (ii) not receiving all of said at least one acknowledgement signal prior to an expiration of said second timer.

10. The method of claim 9, wherein said first and second timers are started simultaneously.

11. The method of claim 10 further comprising the step of receiving a signal indicating that said processor is properly initialized,

wherein said first and second timers are started upon receiving said initialization signal.

12. The method of claim 9, wherein said step of resetting said processor further comprises the step of:

storing state information pertaining to said processor.

13. The method of claim 9, further comprising the step of

starting a boot up timer, and

resetting said processor if an initialization signal is not received from said processor prior to an expiration of said boot up timer, wherein said initialization signal indicates that said processor is properly initialized.

14. The method of claim 13, wherein said first and second timers are simultaneously started upon receiving said initialization signal.

15. A method for resetting a processor coupled to a watchdog comprises the steps of:

monitoring a processor using a watchdog coupled to said processor,

resetting said processor using said watchdog,

storing state information of said processor immediately prior to resetting said processor, wherein said state information indicates a state the processor was in prior to reset.

16. The method of claim 15, wherein said step of storing comprises the step of asserting a nonmaskable interrupt (NMI).

17. A watchdog system for monitoring functionality of a processor, the system comprising:

control logic having N number of acknowledgement signal inputs;

a boot up timer, wherein said boot up timer is started at the start of a boot up of a processor;

a forbidden timer, wherein the said forbidden timer is started upon start of every operational cycle after completion of a successful boot up of said processor,

an acknowledgement timer, wherein said acknowledgement timer is started upon receiving an acknowledgement signal at one of said N number of acknowledgement signal inputs;

a cycle period timer, wherein said cycle period timer is started upon start of every operational cycle after completion of a successful boot up of said processor; and

a reset signal generator.

18.   The watchdog system of claim 17, wherein said reset signal generator generates a reset signal to send to said processor upon any one of the following conditions being met:

(i) not receiving an acknowledgement signal at a first one of said N number of acknowledgement signal inputs before an expiration of said boot up timer, (ii) receiving an acknowledgement signal at any one of said N number of acknowledgement signal inputs before an expiration of said acknowledgement timer; (iii) receiving an acknowledgement signal at any one of said N number of acknowledgement signal inputs before an expiration of said forbidden timer and (iv) not receiving an acknowledgement signal at all of said N number of acknowledgement signal inputs before an expiration of said cycle period timer.

19.   The watchdog system of claim 17, further comprising an interface coupled to said control logic via said N number of acknowledgement signal inputs, wherein said interface couples said processor to said watchdog system.

20.   The watchdog system of claim 19, wherein said reset signal resets said processor coupled to said processor interface.

21.   The watchdog system of claim 20, further includes logic to save information pertaining to a state of said processor immediately prior to reset.

22.   The watchdog system of claim 17, wherein a duration of each of said timers can be set to unique values.

23.   The watchdog system of claim 17, wherein said N number of acknowledgement signal inputs are input/output lines.

24.   The watchdog system of claim 17, wherein said N number of acknowledgement signal inputs are registers.

25.   A method of monitoring the functionality of a processor comprising the steps of:

starting a boot up timer,

starting a forbidden timer;

starting a cycle period timer;

receiving at least one acknowledgement signal;

upon the reception of one of at least one acknowledgement signal, starting an acknowledgement timer; and

resetting said processor if any one of the following conditions are met:

(i) not receiving any one of said at least one acknowledgement signal prior to an expiration of said boot up timer; (ii) receiving any one of said at least one acknowledgement signal prior to an expiration of said acknowledgement timer; (iii) receiving any one of said at least one acknowledgement signal prior to an expiration of said forbidden timer, and (iv) not receiving all of said at least one acknowledgement signal prior to an expiration of said cycle period timer.